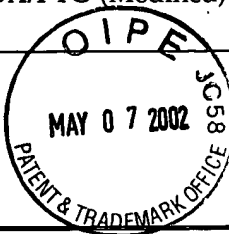



Substitute for Form 1449A/PTO (Modified)		Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 1 of 4	 	First Named Inventor: Jin Yang	Examiner : Unassigned <i>IPS #4</i>
		Filing Date: June 30, 2000	Art Unit: 2763

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
<i>EG</i>		5,469,367		Puri et al	11-21-1995	
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 2 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned <i>IDS # 4</i>
		Filing Date: June 30, 2000	Art Unit: 2763



OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
<i>A</i> <i>EG</i>		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University, January 15, 1997</i>	
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<i>D</i> <i>EG</i>		BRYANT, R. E., "Binary Decision Diagrams & Beyond," Tutorial at ICCAD '95, <i>Carnegie Mellon University, 1995</i>	
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<i>I</i> <i>EG</i>		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University, May 1997</i>	
<i>J</i> <i>EG</i>		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," <i>ACM Transactions on Software Engineering and Methodology, Vol. 8, No. 1, January 1999, pages 49-78</i>	
<i>K</i> <i>EG</i>		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," <i>Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design, November, 1992, pages 172-178</i>	

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Sheet 3 of 4		First Named Inventor: Jin Yang	Examiner: <i>105 # 4</i> Unassigned
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<i>EG</i>		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
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<i>EG</i>		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 16, No. 5, September 1994, pages 1512-1542	
<i>EG</i>		GRUMBERG, O., "Model Checking and Modular Verification," <i>ACM Transactions On Programming Languages and Systems</i> , Vol. 16, No. 3, May 1994, pages 843-871	
<i>EG</i>		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219, Carnegie Mellon University</i> , December 1994	
<i>T</i>		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	

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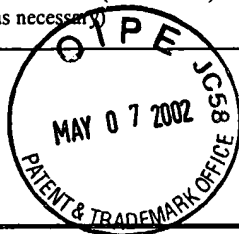
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Sheet 4 of 4		First Named Inventor: Jin Yang	Examiner: <i>IPS #4</i> Unassigned
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<i>U</i> <i>ES</i>		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
<i>V</i> <i>ES</i>		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32nd ACM/IEEE Conference on Design Automation</i> , January 1995	
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<i>X</i> <i>ES</i>		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," <i>ACM Transactions on Design Automation of Electronic Systems</i> , Vol. 4, No. 2, April 1999, pages 123-193	
<i>Y</i> <i>ES</i>		KURSHAN, R. et al, "Verifying Hardware in its Software Context," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 742-749	
<i>Z</i> <i>ES</i>		NELSON, K. L. et al, "Formal Verification of a Superscalar Execution Unit," <i>34th Design Automation Conference</i> , June 1997	
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<i>AB</i> <i>ES</i>		VELEV, M. N., "Efficient Modeling of Memory Arrays in Symbolic Simulations," <i>Proceedings of Computer-Aided Verification</i> , June 1997	
<i>AC</i> <i>ES</i>		WING, J. M. et al, "A Case Study in Model Checking Software Systems," <i>Technical Report CMU-CS-96-124, Carnegie Mellon University, Pittsburgh, PA</i> , April 1996	
<i>AD</i> <i>ES</i>		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28th ACM/IEEE Design Automation Conference</i> , 1991	

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